in a semiconductor layer on a lower surface of the gate insulation layer, a diffusion region formed in the semiconductor substrate; and

source and drain regions comprised of N-type impurity regions formed adjacent to the gate insulation layer and gate electrode,

wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not more than 1.0, where the L_{bc} is a depth of the buried channel region adjacent to a boundary formed by the N-type impurity region and the P-type silicon carbide region, and the X_j is a depth of the source and drain regions.

8. (Amended) A device according to claim 2, wherein the diffusion region has an impurity concentration that is not lower than a maximum impurity concentration of the impurity region used to form the buried channel region and not higher than an impurity concentration of the source or drain regions.

9. (Amended) A device according to claim 7, wherein the diffusion region has an impurity concentration that is not lower than a maximum impurity concentration of the impurity region used to form the buried channel region and not higher than an impurity concentration of the source or drain regions.

10. (Amended) A device according to claim 8, wherein the diffusion region comprises nitrogen, phosphorus, or arsenic at a maximum concentration that is from 5×10^{16} cm^{-3} to 1×10^{19} cm^{-3}.

11. (Amended) A device according to claim 9, wherein the diffusion region

comprises nitrogen, phosphorus, or arsenic at a maximum concentration that is from 5 x 10^{16} cm^{-3} to 1 x 10^{19} cm^{-3}.

12. (Amended) A device according to claim 7, wherein the diffusion region is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel region.

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13. (Amended) A device according to claim 10, wherein the diffusion region is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel region.

14. (Amended) A device according to claim 11, wherein the diffusion region is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel formation region.

15. (Amended) A device according to claim 13, wherein the diffusion region is a high-concentration P-type impurity diffusion region located adjacently under the buried channel region that includes an aluminum or boron diffusion region having a maximum impurity concentration of 1 x 10^{17} cm^{-3} to 1 x 10^{19} cm^{-3}.

16. (Amended) A device according to claim 14, wherein the diffusion region is a